TMC2340A

Digital Synthesizer

Dual 16 Bit, 50 Msps

Features

- User-configurable phase accumulator for waveform synthesis, frequency modulation or phase modulation
- Amplitude input for amplitude modulation and gain adjustment
- Guaranteed 50 Msps pipelined data throughput rate
- 15-bit magnitude, 32-bit phase data input precision
- 16-bit offset binary or 15-bit unsigned magnitude output data format
- Input register clock enables simplify interfacing
- Low power consumption CMOS process
- Single +5V power supply
- Available in a 120-pin plastic pin grid array package (PPGA) and 120-pin metric quad flat pack (MQFP)

Applications

- Digital waveform synthesis, including quadrature functions
- Digital modulation and demodulation

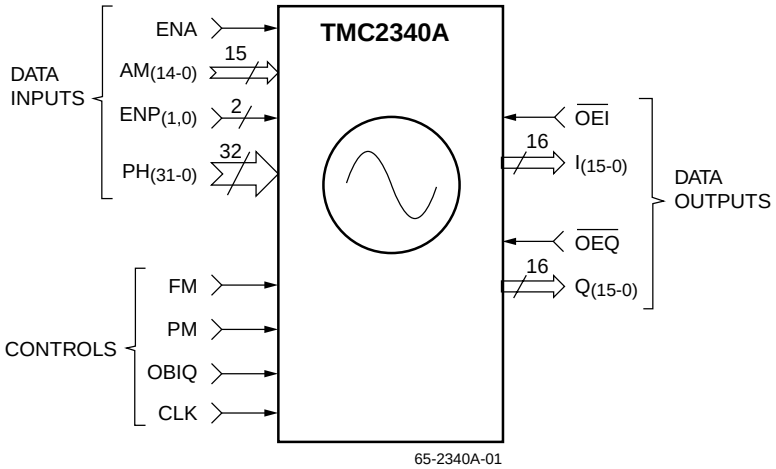
Description

The TMC2340A performs waveform synthesis, modulation, and demodulation. When presented with a TTL clock signal and user-selected 15-bit amplitude and 32-bit phase increment values, the TMC2340A automatically generates quadrature matched pairs of 16-bit sine and cosine waves in DAC-compatible 16-bit offset binary format. If desired, these waveforms are easily phase or frequency-modulated on-chip, and the amplitude input facilitates gain adjustment or amplitude modulation. Digital output frequencies are restricted only by the Nyquist limit of clock rate/2, with frequency resolution of 0.012 Hz at the guaranteed maximum 50 MHz clock rate.

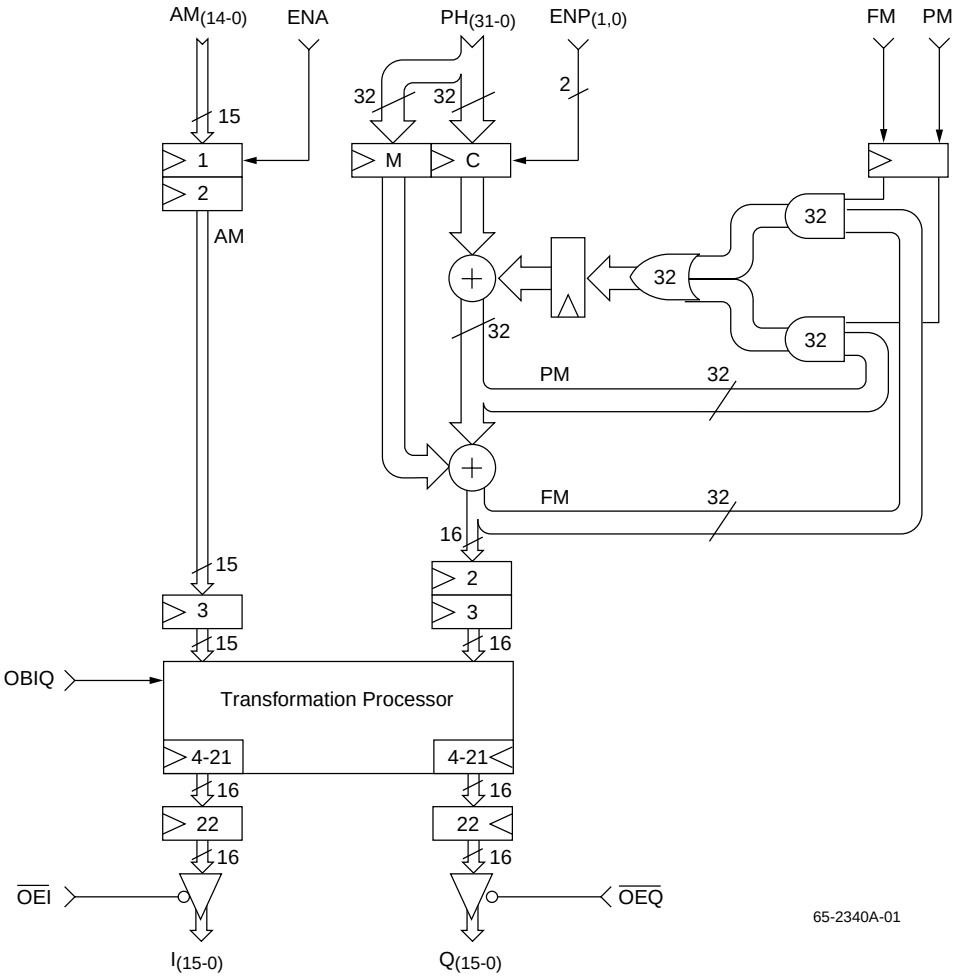
A new data word pair is available at the output every clock cycle. All input and output data ports are registered, with a user-configurable phase accumulator structure and input register clock enables to simplify interfacing. The phase data range over a full 2π radians. All signals are TTL compatible.

Fabricated in a submicron CMOS process, the TMC2340A operates at the 50 MHz maximum clock rate over the full commercial temperature (0 to 70°C) and supply (4.75 to 5.25V) voltage ranges, and is available in low-cost 120 pin plastic pin grid array (PPGA) and a 120-lead metric quad flat pack (MQFP) package.

Logic Symbol



Block Diagram



Functional Description

General Information

The TMC2340A converts Polar (Phase and Magnitude) data into Rectangular (Cartesian) format. The first transformed result is available at the outputs 22 clock cycles after startup, with new output data available every clock cycle. All input and output data ports are registered, with input clock enables to simplify system bus connections.

The input ports accept 15-bit amplitude and 32-bit phase data, and the output ports produce 16-bit Rectangular data words in either 16-bit offset binary or 15-bit unsigned magnitude format. The 32-bit phase accumulator handles high-accuracy (0.012Hz at the maximum clock rate) phase increment values with minimal accumulation error. The flexible input phase accumulator structure supports frequency or phase modulation, as determined by the input register clock enable $ENYP_{1,\ 0}$ and accumulator controls FM and PM. The 16 MSBs (Most Significant Bits) of phase data are used in the transformation itself.

Table 1. Data Input/Output Formats – Integer Format

Port	OBIQ	BIT# 31	30	29	.	.	.	16	15	14	.	.	.	0	Format	
AM	X									2^{14}	.	.	.	2^{0}.		U
PH	X	$\pm2^{0}$	2^{-1}	2^{-2}				2^{-15}	2^{-16}	2^{-17}	.	.	.	2^{-31}	(xπ)	T/U
I	0									2^{14}	.	.	.	2^{0}.		U
I	1								2^{15}	2^{14}	.	.	.	2^{0}.		B
Q	0									2^{14}	.	.	.	2^{0}.		U
Q	1								2^{15}	2^{14}	.	.	.	2^{0}.		B

Notes:

1. $\pm2^{0}$ denotes two's complement sign or highest magnitude bit — since phase angles are modulo 2π and phase accumulator is modulo 2^{32} this bit may be regarded as $\pm\pi$.
2. All phase angles are in terms of π radians, hence notation "xπ."
3. A sign-and-magnitude "Q" output is obtained by appending the input bit PH_{31} as a sign bit to the corresponding (i.e., delayed 22 cycles) Q_{14-0}.
4. A sign-and-magnitude "I" output is obtained by appending the exclusive OR of PH_{31} and PH_{30} as a sign bit to the corresponding I_{14-0}.
5. When OBIQ=0, outputs I_{15} and Q_{15} become "do not connects" and will stay at logic HIGH. (They may be wired to V_{DD}, left open, or connected to any logic input without damage to the part or excessive power consumption.)
6. Formats:
   T/U = Two's Complement/Unsigned Magnitude 32 Bits
   U = Unsigned Magnitude15 Bits
   B = Offset Binary16 Bits

AM, I, Q			PH	
HEX	U	B	T	U
FFFF		32767	$-\pi \cdot 2^{-15}$	$\pi(2-2^{-15})$
– –	– –	– –		
8001		1	$-\pi(1-2^{-15})$	$\pi(1+2^{-15})$
8000		0	$-\pi$	π
7FFF	32767	-1	$\pi(1-2^{-15})$	$\pi(1-2^{-15})$
– –	– –	– –		
0001	1	-32767	$\pi \cdot 2^{-15}$	$\pi \cdot 2^{-15}$
0000	0	-32768	0	0

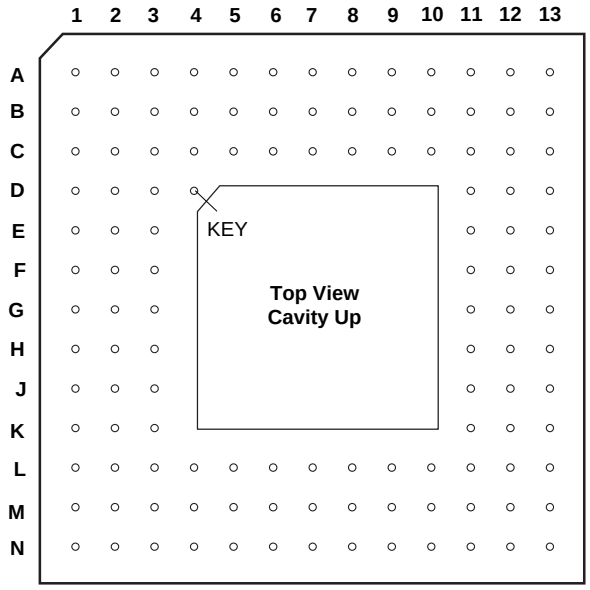
"Hex" column contains the 16 MSBs of the 32-bit phase input (16 LSBs are 0), the 15 bits of the amplitude input or the 16 bits of the offset binary output

Static Control Input

OBIQ determines the numeric format of the output data: offset binary if HIGH and unsigned magnitude if LOW. This control acts with 2-cycle latency on the chip's 22-cycle data path and is normally hardwired to a system-specific state.

Pin Assignments

120-Pin Plastic Pin Grid Array (PPGA)

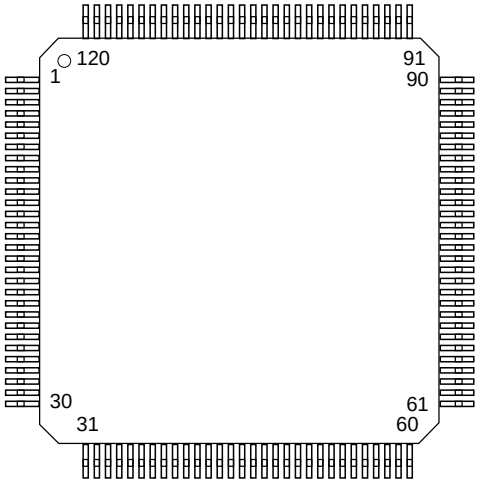


65-2340A-03

Pin	Name	Pin	Name	Pin	Name	Pin	Name
A1	Q_5	C5	GND	G11	GND	L10	PH_{31}
A2	Q_7	C6	V_{DD}	G12	AM_{12}	L11	V_{DD}
A3	Q8	C7	GND	G13	AM_{13}	L12	AM_3
A4	Q_{10}	C8	V_{DD}	H1	PM	L13	AM_4
A5	Q_{12}	C9	GND	H2	FM	M1	PH_6
A6	Q_{14}	C10	GND	H3	V_{DD}	M2	PH_9
A7	Q_{15}	C11	V_{DD}	H11	AM_9	M3	PH_{11}
A8	I_0	C12	I_{11}	H12	AM_{10}	M4	PH_{13}
A9	I_2	C13	I_{13}	H13	AM_{11}	M5	PH_{16}
A10	I_4	D1	$\overline{OEQ}$	J1	PH_0	M6	PH_{18}
A11	I_6	D2	Q_0	J2	PH_1	M7	PH_{20}
A12	I_8	D3	GND	J3	PH_3	M8	PH_{23}
A13	I_{10}	D11	GND	J11	GND	M9	PH_{25}
B1	Q_3	D12	I_{14}	J12	AM_7	M10	PH_{28}
B2	Q_4	D13	I_{15}	J13	AM_8	M11	ENA
B3	Q_6	E1	GND	K1	PH_2	M12	AM_1
B4	Q_9	E2	GND	K2	PH_4	M13	AM_2
B5	Q_{11}	E3	V_{DD}	K3	GND	N1	PH_8
B6	Q_{13}	E11	V_{DD}	K11	GND	N2	PH_{10}
B7	GND	E12	GND	K12	AM_5	N3	PH_{12}
B8	I_1	E13	$\overline{OEI}$	K13	AM_6	N4	PH_{15}
B9	I_3	F1	OBIQ	L1	PH_5	N5	PH_{17}
B10	I_5	F2	GND	L2	PH_7	N6	PH_{19}
B11	I_7	F3	CLK	L3	GND	N7	PH_{21}
B12	I_9	F11	V_{DD}	L4	V_{DD}	N8	PH_{22}
B13	I_{12}	F12	GND	L5	PH_{14}	N9	PH_{24}
C1	Q_1	F13	AM_{14}	L6	V_{DD}	N10	PH_{26}
C2	Q_2	G1	ENP_1	L7	GND	N11	PH_{29}
C3	V_{DD}	G2	ENP_0	L8	V_{DD}	N12	PH_{30}
C4	GND	G3	GND	L9	PH_{27}	N13	AM_0

Pin Assignments (continued)

120-Lead Metric Quad Flat Pack (MQFP)



65-2340A-04

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{DD}	31	GND	61	V_{DD}	91	V_{DD}
2	Q_4	32	PH_9	62	AM_1	92	I_9
3	Q_3	33	PH_{10}	63	AM_2	93	I_8
4	GND	34	V_{DD}	64	GND	94	GND
5	Q_2	35	PH_{11}	65	AM_3	95	I_7
6	Q_1	36	PH_{12}	66	AM_4	96	I_6
7	Q_0	37	PH_{13}	67	AM_5	97	I_5
8	V_{DD}	38	PH_{14}	68	GND	98	GND
9	$\overline{OEQ}$	39	PH_{15}	69	AM_6	99	I_4
10	GND	40	PH_{16}	70	AM_7	100	I_3
11	GND	41	PH_{17}	71	AM_8	101	I_2
12	CLK	42	V_{DD}	72	AM_9	102	V_{DD}
13	GND	43	PH_{18}	73	AM_{10}	103	I_1
14	OBIQ	44	PH_{19}	74	AM_{11}	104	I_0
15	ENP_0	45	PH_{20}	75	AM_{12}	105	GND
16	GND	46	GND	76	GND	106	GND
17	ENP_1	47	PH_{21}	77	AM_{13}	107	Q_{15}
18	PM	48	PH_{22}	78	AM_{14}	108	Q_{14}
19	FM	49	PH_{23}	79	GND	109	Q_{13}
20	V_{DD}	50	V_{DD}	80	V_{DD}	110	V_{DD}
21	PH_0	51	PH_{24}	81	$\overline{OEI}$	111	Q_{12}
22	PH_1	52	PH_{25}	82	GND	112	Q_{11}
23	PH_2	53	PH_{26}	83	I_{15}	113	Q_{10}
24	PH_3	54	PH_{27}	84	V_{DD}	114	GND
25	PH_4	55	PH_{28}	85	I_{14}	115	Q_9
26	PH_5	56	PH_{29}	86	I_{13}	116	Q_8
27	PH_6	57	PH_{30}	87	I_{12}	117	Q_7
28	GND	58	PH_{31}	88	GND	118	GND
29	PH_7	59	ENR	89	I_{11}	119	Q_6
30	PH_8	60	AM_0	90	I_{10}	120	Q_5

Pin Descriptions

Pin Name	Pin Number		Pin Function Description
	PPGA	MQFP	
Power, Ground and Clock			
V_{DD}	C3, E3, H3, L4, L6, L8, L11, F11, E11, C11, C8, C6	1, 8, 20, 34, 42, 50, 61, 80, 84, 91, 102, 110	The TMC2340A operates from a single +5V supply. All power and ground pins must be connected.
GND	D3, E2, E1, F2, G3, K3, L3, L7, K11, J11, G11, F12, E12, D11, C10, C9, B7, C7, C5, C4	4, 10, 11, 13, 16, 28, 31, 46, 64, 68, 76, 79, 82, 88, 94, 98, 105, 106, 114, 118	Ground
CLK	F3	12	The TMC2340A operates from a single clock. All enabled registers are strobed on the rising edge of CLK, which is the reference for all timing specifications.

Pin Descriptions (continued)

Pin Name	Pin Number PPGA	Pin Number MQFP	Pin Function Description
Inputs/Outputs			
AM_{14-0}	F13, G13, G12, H13, H12, H11, J13, J12, K13, K12, L13, L12, M13, M12, N13	78, 77, 75-69, 67-65, 63, 62, 60	AM_{14-0} is the registered peak amplitude 15-bit input data port. AM_{14} is the MSB.
PH_{31-0}	L10, N12, N11, M10, L9, N10, M9, N9, M8, N8, N7, M7, N6, M6, N5, M5, N4, L5, M4, N3, M3, N2, M2, N1, L2, M1, L1, K2, J3, K1, J2, J1	58-51, 49-47, 45-43, 41-35, 33, 32, 30, 29, 27-21	PH_{31-0} is the registered Phase angle increment 32-bit input data port. The input phase accumulators are fed through this port in conjunction with the input enable select $ENP_{1,0}$. PH_{31} is the MSB.
I_{15-0}	D13, D12, C13, B13, C12, A13, B12, A12, B11, A11, B10, A10, B9, A9, B8, A8	83, 85, 86, 87, 89, 90, 92, 93, 95-97, 99-101, 103, 104	I_{15-0} is the registered X-coordinate 16-bit output data port. This output is forced into the high-impedance state when $\overline{OEI}$=HIGH. I_0 is the LSB. I_{15} will be "stuck at" logic HIGH if OBIQ=O.
Q_{15-0}	A7, A6, B6, A5, B5, A4, B4, A3, A2, B3, A1, B2, B1, C2, C1, D2	107-109, 111-113, 115-117, 119, 120, 122, 123, 125-127	Q_{15-0} is the registered Cartesian Y-coordinate 16-bit output data port. This output is forced to the high- impedance state when $\overline{OEQ}$=HIGH. Q_0 is the LSB. Q_{15} will remain at logic HIGH if OBIQ=0.
Controls			
ENA	M11	59	Data presented to the input port AM are latched into the input registers on the current clock when ENA is HIGH. When ENA is LOW, the data stored in the register remains unchanged.
$ENP_{1,0}$	G1, G2	17, 15	The value presented to the PH input port is latched into the phase accumulator input registers on the current clock, as determined by the control inputs $ENP_{1,0}$, as shown below: **$ENP_{1,0}$** / **Instruction** 00 — No registers enabled, current data held 01 — M register input enabled, C data held 10 — C register input enabled, M data held 11 — M register set to 0, C register input enabled where C is the Carrier register and M is the Modulation register, and 0=LOW, 1= HIGH. See the Block Diagram.

Pin Descriptions (continued)

<table>
<tr><th rowspan="2">Pin Name</th><th colspan="2">Pin Number</th><th rowspan="2">Pin Function Description</th></tr>
<tr><th>PPGA</th><th>MQFP</th></tr>
<tr><td>FM, PM</td><td>H2, H1</td><td>19, 18</td><td>The user determines the internal phase Accumulator structure implemented on the next clock by setting the accumulator control word FM, PM, as shown below:

<table><tr><th>FM, PM</th><th>Instruction</th></tr><tr><td>00</td><td>No accumulation performed</td></tr><tr><td>01</td><td>PM accumulator path enabled</td></tr><tr><td>10</td><td>FM accumulator path enabled</td></tr><tr><td>11</td><td>(Nonsensical) logical OR of PM and FM</td></tr></table>
where 0=LOW, 1=HIGH. See the Block Diagram.

The accumulator will roll over correctly when full-scale is exceeded, allowing the user to perform continuous phase accumulation through 2π radians, or 360 degrees.</td></tr>
<tr><td>OBIQ</td><td>F1</td><td>14</td><td>The format select control sets the numeric format of the Rectangular data: offset binary format when HIGH, and unsigned when LOW. This is a static input. See the Timing Diagram.</td></tr>
<tr><td>$\overline{OEI}$, $\overline{OEQ}$</td><td>E13, D1</td><td>81, 9</td><td>Data in the output registers are available at the outputs of the device when the respective asynchronous Output Enables are LOW. When $\overline{OEI}$ or $\overline{OEQ}$ is HIGH, the respective output port is in the high-impedance state.</td></tr>
</table>

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter	Min	Max	Units
Power Supply Voltage (V_{CC})	-0.5	7	V
Input Voltage	-0.5 to (V_{DD}+0.5)V		
Applied Voltage[2] Output	-0.5	V_{DD}+0.5	
Externally Forced Current Output			
Short-circuit Duration Output (single output in HIGH state to ground)		1 second	
Operating Temperature	-20	110	°C
Storage Temperature	-65	150	°C
Junction Temperature		140	°C
Lead Soldering Temperature (10 sec)		300	°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating Conditions

Parameter		Condition	Min	Nom	Max	Units
V_{DD}	Power Supply Voltage		4.75	5.0	5.25	V
f_{CLK}	Clock frequency	TMC2340A			20	MHz
		TMC2340A-1			40	MHz
		TMC2340A-2			50	MHz
t_{PWH}	Clock Pulse Width, HIGH		7			ns
t_{PWL}	Clock Pulse Width, LOW		6			ns
t_S	Input Data Setup Time		6			ns
t_H	Input Data Hold Time		1			ns
V_{IH}	Input Voltage, Logic HIGH		2.0			V
V_{IL}	Input Voltage, Logic LOW				0.8	V
I_{OH}	Output Current, Logic HIGH				-2.0	mA
I_{OL}	Output Current, Logic LOW				4.0	mA
T_A	Ambient Temperature, Still Air		0		70	°C

Electrical Characteristics

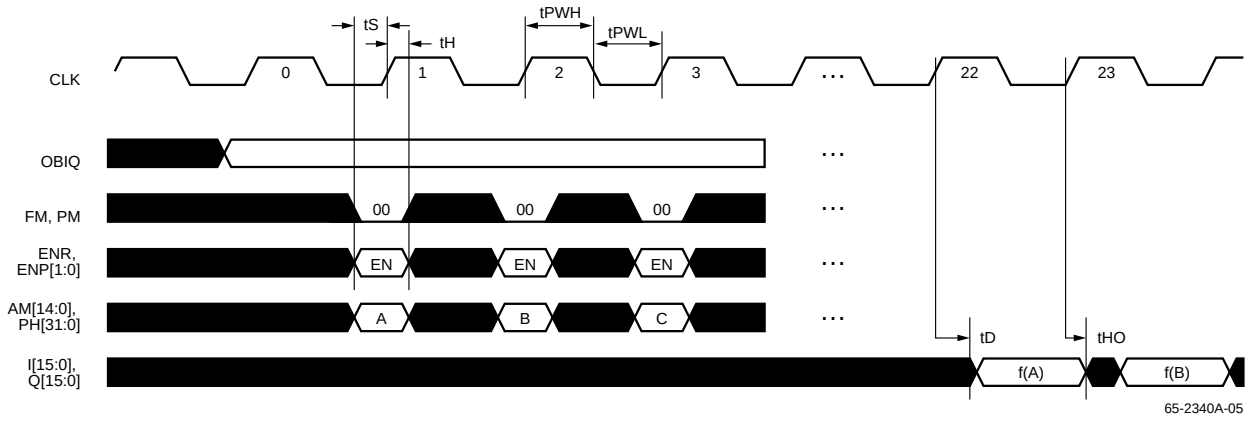
Parameter		Conditions	Min	Nom	Max	Units
I_{DD}	Power Supply Current	V_{DD} = Max, C_{LOAD} = 25pF, f_{CLK} = Max				
		TMC2340A			140	mA
		TMC2340A-1			240	mA
		TMC2340A-2			290	mA
I_{DDU}	Power Supply Current, Unloaded	V_{DD} = Max, $\overline{OEI}$, $\overline{OEQ}$ = HIGH, f_{CLK} = Max				
		TMC2340A			95	mA
		TMC2340A-1			175	mA
		TMC2340A-2			215	mA
I_{DDQ}	Power Supply Current, Quiescent	V_{DD} = Max,CLK = LOW			5	mA
C_{PIN}	I/O Pin Capacitance			5		pF
I_{IH}	Input Current, HIGH	V_{DD} = Max, V_{IN} = V_{DD}			±10	µA
I_{IL}	Input Current, LOW	V_{DD} = Max, V_{IN} = 0 V			±10	µA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD} = Max, V_{IN} = V_{DD}			±10	µA
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD} = Max, V_{IN} = 0 V			±10	µA
I_{OS}	Short-Circuit Current		–20		–80	mA
V_{OH}	Output Voltage, HIGH	I_{OH} = Max	2.4			V
V_{OL}	Output Voltage, LOW	I_{OL} = Max			0.4	V

Switching Characteristics

Parameter		Conditions[1]	Min	Nom	Max	Units
t_{DO}	Output Delay Time	C_{LOAD} = 25 pF			16	ns
t_{HO}	Output Hold Time	C_{LOAD} = 25 pF	3			ns
t_{ENA}	Three-State Output Enable Delay	C_{LOAD} = 0 pF			13	ns
t_{DIS}	Three-State Output Disable Delay	C_{LOAD} = 0 pF			13	ns

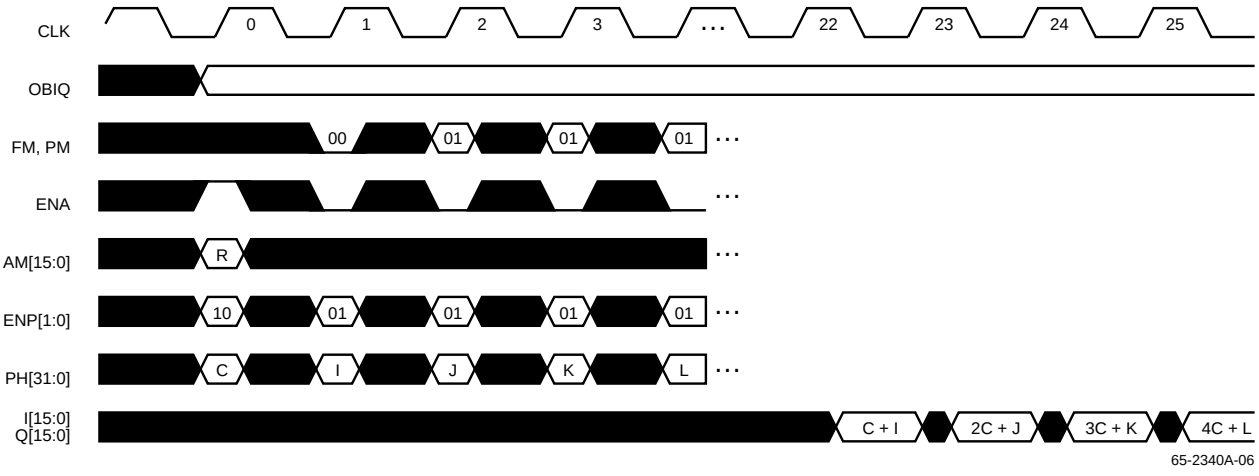
Note:
1. All transitions are measured at a 1.5V level except for t_{ENA} and t_{DIS}.

Timing Diagram – No Accumulation



Note: $\overline{OEI}$, $\overline{OEQ}$ = LOW.

Timing Diagram – Phase Modulation



Notes:
1. $\overline{OEI}$, $\overline{OEQ}$ = LOW.
2. Carrier C and peak amplitude A loaded on CLK 0.
3. Modulation values I, J, K, L, ... loaded on CLK 1, CLK 2, etc.
4. Output corresponding to modulation loaded at CLK i emerged t_{DO} after CLK i +21.
5. To modulate amplitude, vary AM with ENA = 1.

Equivalent Circuits and Transition Levels

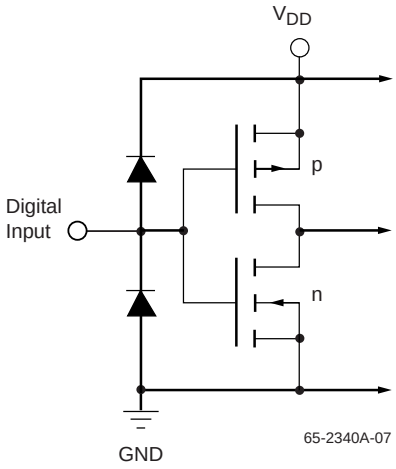


Figure 1. Equivalent Input Circuit

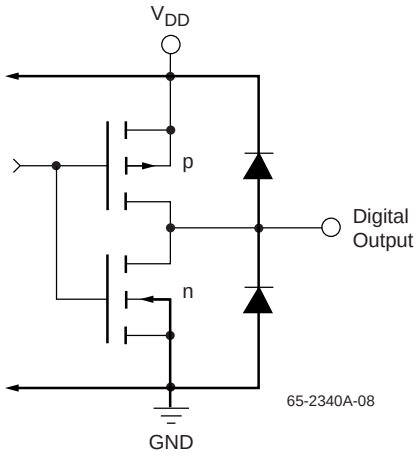


Figure 2. Equivalent Output Circuit

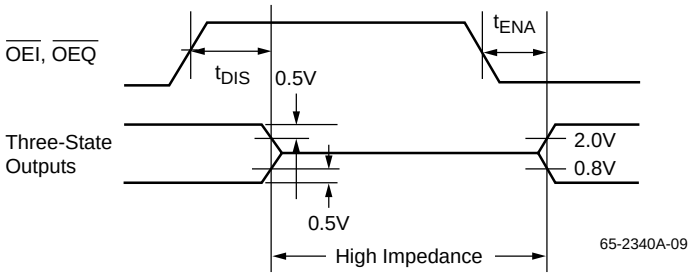


Figure 3. Transition Levels for Three-State Measurements

Digital Waveform Synthesis

Generating Unmodulated Sine and Cosine Waves

The TMC2340 can generate simultaneous quadrature-matched sine and cosine waves with optional amplitude, frequency, or phase modulation. To obtain an unmodulated waveform, the user loads the desired phase step value, computed as:

$$f_C = \frac{2^{32} \times \text{desired\_output\_frequency}}{\text{digital\_clock\_frequency}}$$

into the 32-bit-wide carrier register via the PH input port, and applies the desired sinusoid amplitude (half of the desired peak-to-peak value) to the 15-bit-wide AM input port. As the chip's internal phase accumulator increments linearly in steps of f_C, the chip will output a series of complex number pairs representing the horizontal and vertical projections of a vector rotating about the origin, i.e., cosine and sine waves.

A procedure that will yield continuous unmodulated sinusoids is shown in Table 2.

Table 2. Generating unmodulated sinusoids

FM	PM	ENA	AM	ENP	PH	
0	0	1	a	11	f_C	loads freq & amplitude
0	1	0	x	00	x	starts synthesizer @ phase = f_C
0	1	0	x	00	x	continues @ phase = $2f_C$

Because the chip's internal pipeline is 22 registers deep, the effects of any given set of data inputs or instructions won't be seen for 22 clock cycles. After the (22+n)th rising edge of the system clock, the outputs will be (Figure 4):

$$I(22 + n) = a\cos(2\pi n f_C/2^{32}) \text{ and}$$

$$Q(22 + n) = a\sin(2\pi n f_C/2^{32}),$$

where a is the (constant) amplitude and f_C is the (constant) carrier phase step or frequency ratio. For example, if we arbitrarily set a=4000h and f_C=2000 0000h, the chip will generate quadrature-matched sines and cosines at 1/8 of the clock frequency and 1/2 of full-scale amplitude. Here, the internal phase accumulation sequence will be:

Phase Accumulator	Phase
2000 0000h	45 degrees
4000 0000h	90
6000 0000h	135
8000 0000h	180
a000 0000h	225
c000 0000h	270
e000 0000h	315
0000 0000h	0
2000 0000h	45
• • •	• • •

On any given clock cycle, the phase angle into the chip's polar-to-rectangular converter core is that of the phase accumulator:

$$\text{phase}(n) = nf_C$$

[The maximum possible output frequency is just less than half of the clock rate, per the Nyquist limit. For f>8000 0000, one obtains "negative" frequencies, because the phase increment now aliases backward. Thus, a=4000h and f=e000 0000h will generate a cosine wave and a negated sine wave at 1/8 of the clock frequency and 1/2 of full-scale amplitude.]

Amplitude Modulation

By holding amplitude enable pin ENA high, the user can vary the incoming amplitude sample by sample, thereby amplitude-modulating the output signals. The output equations become:

$$I(22 + n) = a(n) \times \cos(2\pi n f_C/2^{32}) \text{ and}$$

$$Q(22 + n) = a(n) \times \sin(2\pi n f_C/2^{32}),$$

Most amplitude modulation applications employ an external adder to combine a fixed (unsigned magnitude) carrier amplitude with a sample-by-sample two's complement modulation term, such that the chip sees:

$$a(n) = \text{carrier\_amplitude} + \text{amplitude\_modulation}(n)$$

[Since the chip accepts only nonnegative amplitudes, this simple implementation is limited to 100% modulation, wherein the instantaneous incoming amplitude can drop to 0, but not below.]

Again, on any given clock cycle, the phase angle into the chip's polar-to-rectangular converter core is that of the phase accumulator:

$$\text{phase}(n) = nf_C$$

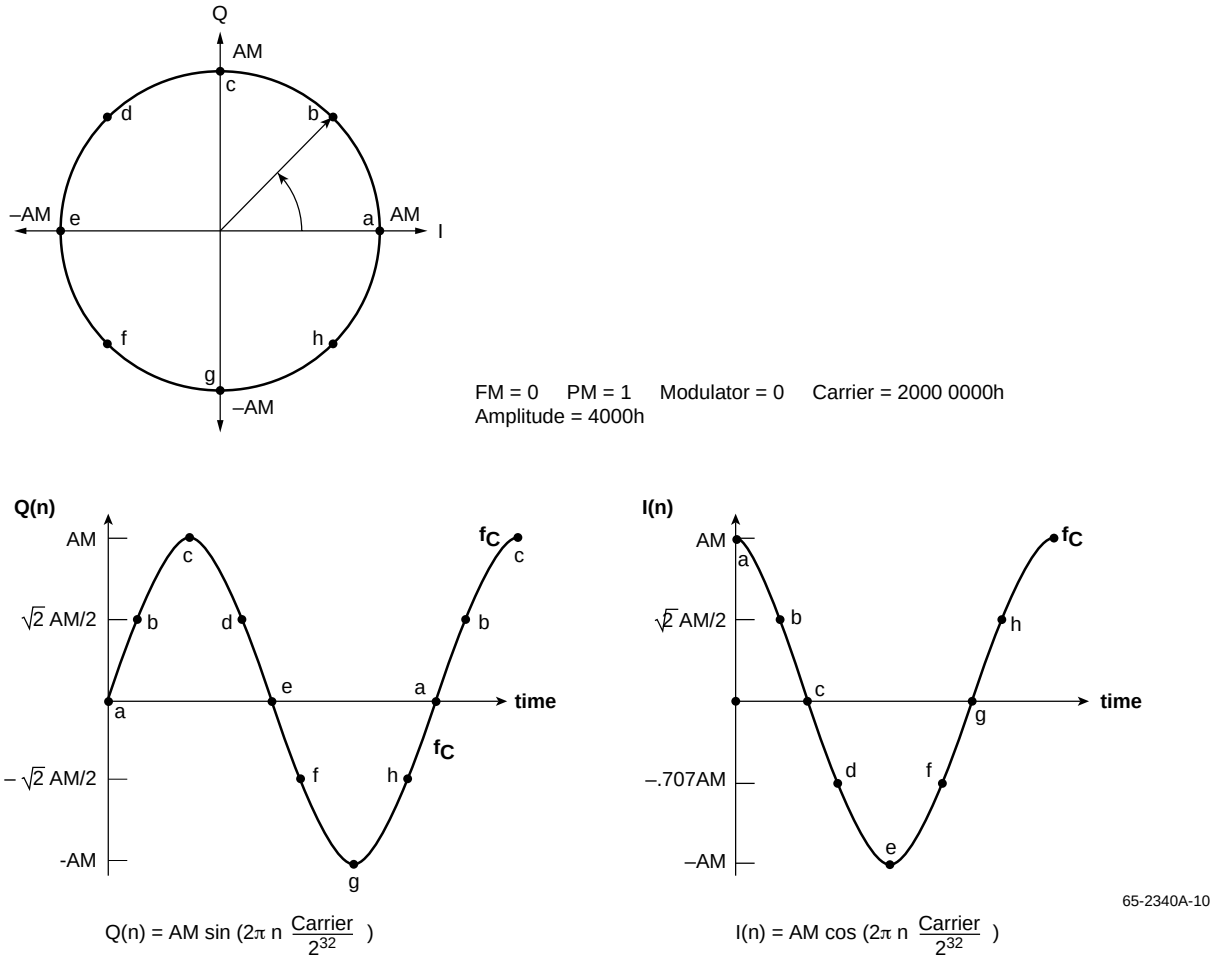


Figure 4. Unmodulated Sinusoid Generation

Phase Modulation

By setting ENP to 10 instead of 00 (while keeping FM = 0 and PM = 1), the user can load a new modulating phase shift into the PH port on each clock cycle. If we label this modulating term p(n), the output equations become:

$I(n+22) = a(n) \times \cos(2\pi(p(n)+nf_C)/2^{32}$

$Q(n+22) = a(n) \times \sin(2\pi(p(n)+nf_C)/2^{32}$

Figure 5 depicts the internal subsarrier architecture in this mode. If we again load carrier = 2000 0000h, but now alternately apply phase modulation (p) terms 0 and 1000 000h, the internal phase sequence will be:

Phase Modulation	Phase
2000 0000h	normal unmodulated start
5000 0000h	phase advanced by an additional 1000 0000h
6000 0000h	phase back to normal progression
9000 0000h	phase advanced by an additional 1000 0000h
a000 0000h	phase back to normal progression
d000 0000h	phase advanced by an additional 1000 0000h
e000 0000h	phase back to normal progression

Here, on any given clock cycle, the phase angle into the chip's polar-to-rectangular converter core is that of the phase accumulator, plus the current value of the modulator:

$phase(n) = nf_C + p(n)$

Frequency Modulation

By setting ENP = 10, FM = 1 , and PM = 0, the user can load a new frequency modulation sample into the PH port on each clock cycle. In phase modulation, the angular modulation term was outside of the phase accumulator/integration loop.

Therefore, each modulation sample affected only a single complex output sample. In frequency modulation, since the angular modulation occurs within the phase accumulator, each modulation sample affects all future outputs. Figure 5 depicts the phase accumulator architecture in this mode.

Consider the following phase advance sequence, using the same 2000 0000h carrier and alternate 0 and 1000 000h modulation, this time in frequency modulation instead of phase modulation mode:

Phase Accumulator	Phase
2000 0000h	unmodulated
5000 0000h	phase advanced by 10000000+20000000
7000 0000h	unmodulated—phase advanced by 20000000
a000 0000h	phase again advanced by 30000000
c000 0000h	advance by 20000000
f000 0000h	advance by 30000000

Here, on any given clock cycle, the phase angle into the chip's polar-to-rectangular converter core is that of the previous cycle, plus carrier + modulator:

$$phase(n+1) = phase(n) + f_C + p(n)$$

and is the same as the present value in phase accumulator. In frequency modulation mode, introducing a single nonzero modulation term will shift the phases of all outputs which follow. In contrast, in phase modulation, introducing a single nonzero modulation term will shift the phase of only one output.

Digital Synthesizer with the TDC1012 D/A Converter

The TDC1012 is an ideal D/A converter for digital synthesis, exhibiting a Spurious-Free Dynamic Range of greater than 70dB. Connection between the TMC2340A and TDC1012 is straightforward, as illustrated in Figure 5.

Either the I or the Q output of the TMC2340 may be connected to the D/A; two converters are used for quadrature synthesis. The trans-former-coupled output circuit shown is recommended for minimum distortion. See the TDC1012 datasheet for details.

Control of the TMC2340A

The TMC2340A needs to be initialized to tell it what frequency and amplitude sinusoid to generate. To initialize amplitude, apply the desired full-scale amplitude to the AM input port of the TMC2340A (AM_{14} through AM_0) and pull ENA HIGH for one clock cycle. This will load the amplitude. If ENA is held HIGH, then the amplitude will follow

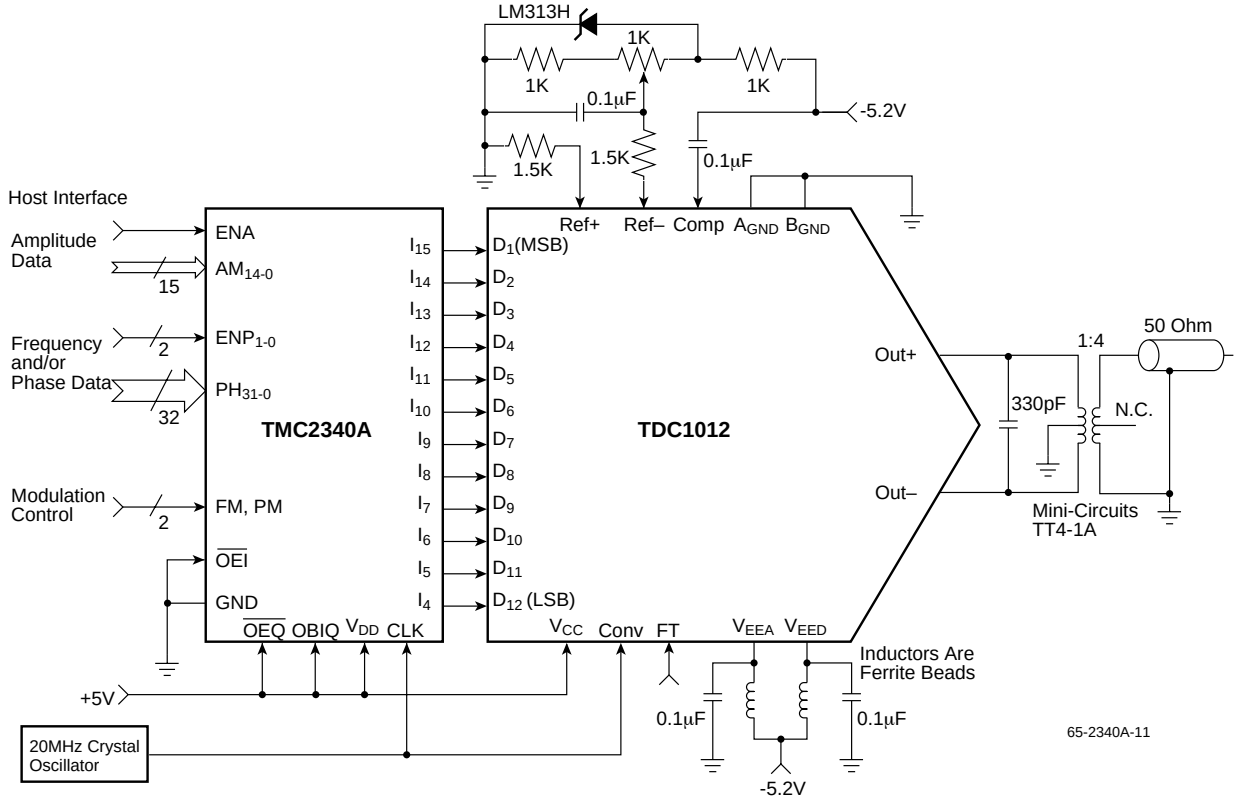


Figure 5. Frequency Synthesizer

the inputs on the AM port. If the user assumes an implied binary point before the MSB of the AM port, the input range will be 0 to just under 1, and the outputs will fall between 0 and 2, with binary points after I_{15} and Q_{15}.

To set the frequency, the C register must be loaded with a value which is the phase increment per clock cycle. If the binary point is considered to be just left of the MSB (input range is 0 to almost 1) then the output frequency is the TMC2340A clock frequency multiplied by the number loaded into C. Since C is 32 bits wide, with a 20MHz clock, one LSB represents a frequency increment of 0.005Hz.

To load the C register, set $ENYP_1$=1 and $ENYP_0$=0; the data presented at the PH port will be loaded on the next clock rising edge.

At this point the TMC2340A has been initialized and can be put into one of three modes depending upon the states of FM and PM:

Mode 0 FM = 0, PM = 0
In this mode the chip is in standby. The unchanging output corresponds to AM cos(PM) on the I outputs with PM being the phase increment.

Mode 1 FM=1, PM=0
Frequency Modulation Mode. The chip generates an output signal of peak amplitude AM and frequency determined by accumulating the sum of the phase increment values in the C and M registers (more about the M register in a later section).

Mode 2 FM=0, PM=1
Phase Modulation Mode. The TMC2340A generates a sinusoid of the frequency represen-ted in the C register and the peak amplitude in the AM register. On each clock cycle, the phase of the signal is offset by the value in the M register. Use this mode with ENP=00 for unmodulated sinewave synthesis.

Modulation

The output of the TMC2340A can be phase (Mode 2) or frequency (Mode 1) modulated. An unmodulated sinusoid results if the contents of registers C and M are held constant. Its frequency is set by C (Mode 2) or C+ M (Mode 1). Since the state of the M register is not defined at power up, the M register should be loaded or cleared to begin operation.

If the signal is to be frequency modulated then the modulation signal is loaded into the M register. The format for the frequency is the same as that for the C register.
If $ENYP_{1,0}$ = 0, 1 then the data value present at the PH port is automatically loaded on each clock rising edge.

For phase modulation, the phase deviation is loaded into the M register (same manner as for frequency modulation). The units of the phase offset are cycles and full-scale is just under one output cycle per TMC2340A clock cycle. The MSB represents a phase of 180°, and the LSB a phase of about $8x10^{-8}$ degrees (eight one-hundred millionths of a degree) or $\pi/2^{31}$ radians.

To synchronize two TMC2340As, first load them with their respective data in mode 0, then switch them simultaneously to either Mode 1 or Mode 2.

Calculating Frequency, Amplitude, and Phase Input Values for the TMC2340A

This Application Brief discusses equations which simplify the calculation of register values which control the TMC2340A. These values allow the generation of output carrier frequency, frequency or phase modulation, and output amplitude.

The results of the equations are converted to binary register values and should be rounded to the resolution of the applicable register (32 or 15-bits). For negative values of phase or frequency modulation, use these equations for positive values and see Table 1 to convert them to negative values.

The TMC2340A operates by continuously incrementing a register (phase accumulator) that rolls over when it becomes full. For example, if the next increment to the phase accumulator causes it to overflow by 47 LSBs, the phase accumulator retains the value 47. The value present in the carrier register (C) is the amount by which the phase accumulator is incremented each system clock cycle. As the value of the carrier register is increased, the value with which the phase accumulator is incremented each clock cycle is increased, resulting in an increased carrier frequency.

The magnitude of the carrier is determined or modulated by the value loaded In the AM register. Phase modulation is accomplished by adding the value of the phase accumulator to the value of the modulation (M) register. This adds an offset to the phase of the carrier. This does not affect the increment value of the phase accumulator and therefore affects only the phase of the carrier, leaving the frequency constant.

Adding the value of the modulation register to the phase accumulator along with the value of the carrier register on each clock cycle results in a shift in frequency. This is because the phase accumulator is incremented by a different amount each clock cycle.

Frequency or phase modulation is selected with the FM and PM input pins which configure the TMC2340A. The equations presented herein are useful for setting carrier frequency and phase, output amplitude, and frequency and phase modulation. To modulate the carrier with an external signal, the signal must be digitized and those values loaded into the modulation inputs of the TMC2340A.

The carrier and modulation registers are loaded through the PH_{31-0} inputs. The $ENP_{1,0}$ inputs select the desired register. The amplitude register is loaded through the AM_{14-0} inputs.

CARRIER FREQUENCY:

$$\text{Carrier Register (C) Value} = \frac{\text{Desired Carrier Frequency}}{\text{Clock Frequency}} \times 2^{32}$$

AMPLITUDE AND AMPLITUDE MODULATION:

$$\text{AM Register Value} = \frac{\text{Desired Output Amplitude}}{\text{Full-Scale Output Amplitude}} \times (2^{15} - 1)$$

FREQUENCY MODULATION:

$$\text{Modulation Register (M) Value} = \frac{\text{Desired Change in Carrier Frequency}}{\text{Clock Frequency}} \times 2^{32}$$

PHASE-MODULATION:

$$\text{Modulation Register (M) Value} = \frac{\text{Desired Change in Phase in Radians (Degrees)}}{2\pi(360°)} \times 2^{32}$$

EXAMPLE 1: Set carrier frequency to 3.579545 MHz with a system clock of 20MHz.

$$\text{Carrier Register (C) Value} = \frac{\text{Desired Carrier Frequency}}{\text{Clock Frequency}} \times 2^{32} = \frac{3.579545 \times 10^6}{20 \times 10^6} \times 2^{32}$$

C = 0.17897725 X 4,294,967,296 = 768,701,436 = 2DD1 73FCh
= 0010 1101 1101 0001 0111 0011 1111 1011 = PH_{31-0}

EXAMPLE 2: Set output amplitude to be 12.2% of full-scale.

$$\text{AM Register Value} = \frac{\text{Desired Output Amplitude}}{\text{Full-Scale Output Amplitude}} \times (2^{15} - 1) = \frac{12.2}{100.0} \times 32767$$

AM = 3,998 = 0F9Eh = 0001 1111 0011 1100 = AM_{14-0}

EXAMPLE 3: Change carrier frequency by 10kHz with a system clock of 3 MHz.

$$\text{Modulation Register (M) Value} = \frac{\text{Desired Change in Carrier Frequency}}{\text{Clock Frequency}} \times 2^{32}$$

$$M = \frac{10 \times 10^3}{3 \times 10^6} \times 2^{32} = 14,316,558 = 00DA\ 740Eh$$

M = 0000 0000 1101 1010 0111 0100 0000 1110 = PH_{31-0}

EXAMPLE 4: Advance the phase of any carrier frequency by 12°.

$$\text{Modulation Register (M) Value} = \frac{\text{Desired Change in Phase}}{360°} \times 2^{32} = \frac{12}{360} \times 2^{32}$$

M = 0.033333 X 2^{32} = 143,165,577 = 0888 8889h
= 0000 1000 1000 1000 1000 1000 1000 1001 = PH_{31-0}

Notes:

Notes:

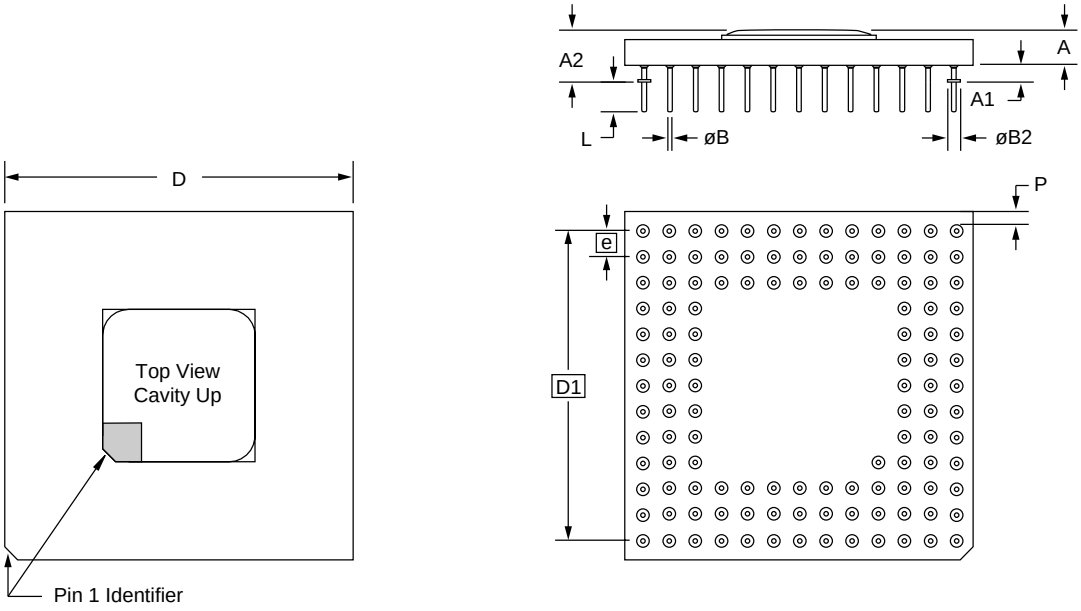
Mechanical Dimensions

121-Pin PPGA Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.080	.160	2.03	4.06	
A1	.040	.060	1.01	1.53	
A2	.125	.215	3.17	5.46	
øB	.016	.020	0.40	0.51	2
øB2	.050 NOM.		1.27 NOM.		2
D	1.340	1.380	33.27	35.05	SQ
D1	1.200 BSC		30.48 BSC		
e	.100 BSC		2.54 BSC		
L	.110	.145	2.79	3.68	
L1	.170	.190	4.31	4.83	
M	13		13		3
N	120		120		4
P	.003	—	.076	—	

Notes:

1. Pin #1 identifier shall be within shaded area shown.
2. Pin diameter excludes solder dip finish.
3. Dimension "M" defines matrix size.
4. Dimension "N" defines the maximum possible number of pins.
5. Orientation pin is at supplier's option.
6. Controlling dimension: inch.



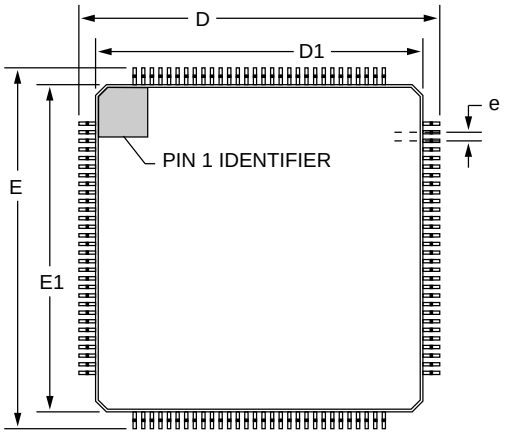
Mechanical Dimensions (continued)

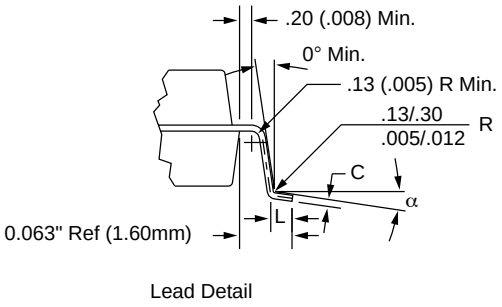
120-Lead MQFP Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.154	—	3.92	
A1	.010	—	.25	—	
A2	.125	.144	3.17	3.67	
B	.012	.018	.30	.45	3, 5
C	.005	.009	.13	.23	5
D/E	1.219	1.238	30.95	31.45	
D1/E1	1.098	1.106	27.90	28.10	
e	.0315 BSC		.80 BSC		
L	.026	.037	.65	.95	4
N	120		120		
ND	30		30		
α	0°	7°	0°	7°	
ccc	—	.004	—	.10	

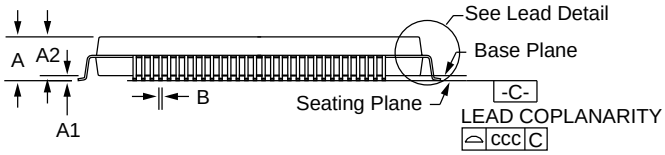
Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Controlling dimension is millimeters.
3. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be .08mm (.003in.) maximum in excess of the "B" dimension. Dambar cannot be located on the lower radius or the foot.
4. "L" is the length of terminal for soldering to a substrate.
5. "B" & "C" includes lead finish thickness.





Lead Detail



Ordering Information

Product Number	Temperature Range	Speed Grade	Screening	Package	Package Marking
TMC2340AH5C	0° to 70°C	20 MHz	Commercial	121-Pin Plastic Pin Grid Array	2340AH5C
TMC2340AH5C1	0° to 70°C	40 MHz	Commercial	121-Pin Plastic Pin Grid Array	2340AH5C1
TMC2340AH5C2	0° to 70°C	50 MHz	Commercial	121-Pin Plastic Pin Grid Array	2340AH5C2
TMC2340AKEC	0° to 70°C	20 MHz	Commercial	120-Pin Metric Quad FlatPack	2340AKEC
TMC2340AKEC1	0° to 70°C	40 MHz	Commercial	120-Pin Metric Quad FlatPack	2340AKEC1
TMC2340AKEC2	0° to 70°C	50 MHz	Commercial	120-Pin Metric Quad FlatPack	2340AKEC2